CLAIMS

1. An enable propagation control circuit comprising:

control logic receiving a plurality of control signals, a reference clock signal and a trigger signal and generating a plurality of pass through control signals; and

a plurality of logic gates, each receiving one of the plurality of pass through control signals and an input enable signal and generating an output enable signal equivalent in logical value to the input enable signal when activated.

2. The enable propagation control circuit of claim 1, wherein receiving a plurality of control signals includes receiving a mode control signal, wherein the mode control signal determines whether the enable propagation control circuit operates in a sequence manager mode or a transparent mode.

3. The enable propagation control circuit of claim 2, wherein the sequence manager mode causes the plurality of pass through control signals to activate each of a portion of the plurality of logic gates in a sequence and for a duration.

4. The enable propagation control circuit of claim 2, wherein the transparent mode causes the plurality of pass through control signals to simultaneously activate all of the plurality of logic gates.

5. The enable propagation control circuit of claim 3, wherein the sequence and the duration are predetermined.

6. The enable propagation control circuit of claim 3, wherein the portion is determined by one of the plurality of control signals.

7. The enable propagation control circuit of claim 3, wherein the sequence and the duration are determined according to the plurality of control signals constrained by internal logic.

8. A transceiver integrated circuit device comprising:

a programmable memory receiving and storing a plurality of control signals and a plurality of enable signals;

an enable propagation control circuit comprising control logic receiving the plurality of control signals from the programmable memory, a reference clock signal and a trigger signal and generating a plurality of pass through control signals; and a plurality of logic gates, each receiving one of the plurality of pass through control signals and an input enable signal from the plurality of enable signals and generating an output enable signal equivalent in logical value to the input enable signal when activated; and

a plurality of sub-blocks, each corresponding to one of the plurality of logic gates and receiving the output enable signal associated with the one of the plurality of logic gates.

9. A method comprising:

receiving a plurality of control signals, a plurality of enable signals, a clock signal and a trigger signal;

in a sequence manager mode, upon receiving the trigger signal, allowing each of a portion of the plurality of enable signals to pass through to their

respective destinations in a sequence and for a duration; and

in a transparent mode, allowing all of the plurality of enable signals to pass through to their respective destinations.

10. The method of claim 9, wherein the sequence manager mode and the transparent mode are determined by one of the plurality of control bits.

11. The method of claim 9, wherein the portion, the sequence, and the duration are determined by the plurality of control bits constrained by logic circuitry.

12. An integrated circuit comprising

a plurality of control inputs receiving a plurality of control signals;

a plurality of enable inputs receiving a corresponding plurality of enable signals;

a plurality of enable outputs delivering a plurality of enable outputs;

a clock input receiving a clock signal; and

a trigger input receiving a trigger signal, wherein the circuit, in a first mode and upon receiving the trigger signal, propagates each of a portion of the plurality of enable signals to a respective enable output in a sequence and for a duration, and wherein the circuit, in a second mode, propagates all of the plurality of enable signals to their respective enable outputs.

13. The circuit of claim 12 wherein the portion is determined by one of the plurality of control signals.

14. The circuit of claim 12, wherein the sequence and duration are determined by a portion of the plurality of control signals constrained by logic circuitry.

15. The circuit of claim 12, wherein the first mode and the second mode are determined by one of the plurality of control signals.